Kishore Damam

FPGA Design Engineer

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PROFESSIONAL SUMMARY

Over 7 years of experience in the field of FPGA design, managing conceptualization, design, and review of FPGA generic/custom products and expansion bring-up. Hands-on experience in all phases of the FPGA module development cycle — requirement gathering, detailed design, RTL coding/ASIC code porting, testbench coding, prototype testing and documentation. Exposure to pre-silicon validation and SoC integration activities. Mentored teams, delegated project sections and steered projects to completion.

KEY SKILLS

- Expertise in FPGA Design
- Extensive experience in VHDL and Verilog RTL and testbench coding
- Expertise in high-speed interfaces like DDR2/3/4, PCI Express, SPI, I2C, Ethernet (10/100/1000), DisplayPort etc.
- Experience in Xilinx, Lattice and Microchip devices
- Expertise in Xilinx, Lattice and Microchip implementation/debugging tools
- Expertise in QuestaSim, ModelSim and Xilinx simulation tools
- Experience in Batch, Tcl, shell scripting and Python
- Experience in pre-silicon validation — bare-metal testing and debugging
- Knowledge of the fundamentals of UVM
- Proficient in technical documentation
- Skillful in debugging technical issues in simulation as well as on board
- Adept in technical as well as team management activities for project execution

Devices	Versal VP1502, Virtex UltraScale+ VU13P, Artix-7, Kintex-7, Spartan-7, Zynq-7000, Spartan-6, Spartan-3, ECP5, PolarFire, PolarFire SoC
Design Tools	Xilinx Vivado, Xilinx ISE, ARM Development Studio, Microchip Libero SoC, Lattice Diamond
On-board Debugging	Chipscope, Vivado Analyzer, DStream-ST
Simulation Tools	QuestaSim, ModelSim, Xilinx Vivado simulator

RELEVANT PROJECTS

Project 1: FPGA Regex Pattern Matching Accelerator (PoC)

Proof of concept RTL for high-throughput Regular Expression matching on network packets, using a split forward/reverse DFA approach on an AMD Xilinx Versal device.

- Top-level architectural design, IP-level RTL coding, and block-level simulation.
- Ran simulations (UVM) and debugged issues using QuestaSim.
- Code integration, synthesis, STA, timing closure of the design.
- On-board testing: bring-up and design validation.

Project 2: Pre-Silicon Validation of ARM Cortex-M85 based SoC

Timing closure of multiple revisions of the design, build-time reduction, LINT checks and on-board validation.

- On-board validation for multiple revisions of the SoC and documentation of the results.
- Memory porting, simulating all test cases and validation of the ported modules.
- Python scripts for insertion of ILA in the implementation flow and for consolidation of LINT reports/checks.
- Bare-metal & disassembly debug with ARM DStream-ST.

Project 3: RISC-V SoC Based Design

Generation of RISC-V (Rocket Chip) SoC design and IP stitching of serial (UART, SPI, I2C and so on) interfaces using an AXI4-Lite backbone interconnect bus. Simulation and SoC-level signal tracing for system-level debugging.

- Top-level architectural design, IP-level RTL coding, synthesis, and block-level simulation.
- Ran simulations (UVM) and debugged issues using QuestaSim.
- Performed SoC-level signal tracing and bus activity analysis to debug data flow across modules.

Project 4: FPGA Generic Board/Module Bring-Up

Conceptualization, design, review and release of new FPGA-based generic/ASIC products.

- FPGA design, coding, simulation, synthesis, implementation and on-board testing for board bring-up.
- Sample RTL-based projects coding, or soft-processor based embedded application projects, testing, review and release.
- Documentation of user manuals, getting-started articles and other board-supporting files.
- Led team in detailed design, coding, simulation, synthesis and board bring-up.

Project 5: ADC Data Acquisition via PCI Express

Design and develop a DAQ solution with 1MSPS ADC data and read the data on a Linux host via PCI Express.

- High-level design of RTL and testbench.
- Detailed RTL design, verification plan generation, testbench design, coding, functional and timing verification, implementation, shell scripting and documentation.

Project 6: Automation Testing

A user-friendly GUI-based solution for peripheral testing of generic FPGA modules.

- Python coding for creation of a GUI-based application using Tkinter for the front end.
- Python coding using Migen (FHDL) for creation of gateware and firmware, migrating gateware for different FPGAs, documentation & blog post with details on building steps and demonstration of running the firmware on the FPGAs.

EDUCATIONAL QUALIFICATION

Qualification	Specialization	Institution
Bachelor of Technology (B.Tech)	Electronics & Communication	Visvesvaraya Technological University, Karnataka, India